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Gate Driver IC with Fully Integrated Overcurrent Protection Function by Measuring Gate-to-Emitter Voltage During IGBT Conduction

Haifeng Zhang[1], Dibo Zhang[1], Hiromu Yamasaki[1], Katsuhiro Hata[1], Keiji Wada[2], Kan Akatsu[3], Ichiro Omura[4], and Makoto Takamiya[1]
[1] The University of Tokyo, Tokyo, Japan
[2] Tokyo Metropolitan University, Tokyo, Japan
[3] Yokohama National University, Kanagawa, Japan
[4] Kyusyu Institute of Technology, Fukuoka, Japan

***Abstract*—To achieve low-cost overcurrent protection for IGBTs without using external components such as high-voltage diodes, a gate driver IC with a fully integrated overcurrent protection function by measuring gate-to-emitter voltage (V_{GE}) during IGBT conduction is proposed. In the proposed gate driver IC, while the IGBTs are ON, constant gate charge is periodically discharged and charged, and when V_{GE} dropped by each discharge is less than the reference voltage, it is detected as the overcurrent and the IGBTs are immediately turned off to protect from the overcurrent. In a single-pulse test of an inductive load at 300 V for an IGBT with a pulse rating of 200 A, the proposed gate driver IC fabricated with 180-nm BCD process successfully protected the overcurrent of 370 A with the protection delay of 810 ns.**

Keywords— overcurrent, protection, gate driver, IC, gate voltage, IGBT

I. Introduction

The detection and protection of IGBT overcurrent are important technologies to realize reliable power electronic systems. The target of this work is to develop a gate driver IC with a fully integrated overcurrent protection function while IGBTs are ON for large-current, short-pulse current generator circuits with inductive load [1] to achieve low-cost overcurrent protection for IGBTs without using external components such as high-voltage diodes.

Methods for detecting overcurrent by measuring collector current (I_C) [2-5], collector-to-emitter voltage (V_{CE}) [3, 6], and gate-to-emitter voltage (V_{GE}) [7-10] of IGBTs have been proposed. I_C measurement requires a current sensor, and V_{CE} measurement for desaturation detection requires a high-voltage diode, which are expensive. All conventional overcurrent detection methods by V_{GE} measurement [7-10] have the disadvantage that overcurrent during ON of IGBTs cannot be detected because V_{GE} is measured during the turn-on transient.

In [11], an overcurrent detection method by "monitoring gate voltage while periodically repeating discharging and charging of constant gate charge (MGDC)" was proposed. In MGDC, while the IGBTs are ON, constant gate charge (Q_C) is periodically discharged and recharged, and when V_{GE} dropped by each discharge is less than the reference voltage (V_{REF}), it is detected as the overcurrent. In [11], however, neither overcurrent detection nor overcurrent protection functions are implemented. In addition, MGDC in [11] is not practical, because it requires many measuring instruments such as a high-speed digital signal generator for timing control of the discharging and the recharging and an oscilloscope to detect V_{GE} drop. To solve the problems, in this paper, a gate driver IC that fully integrates all the functions required for MGDC is proposed, thereby achieving overcurrent protection at low cost.

II. Proposed Gate Driver IC with Fully Integrated Overcurrent Protection Function

Fig. 1 shows an operation principle of the proposed gate driver IC with a fully integrated overcurrent protection function by measuring gate-to-emitter voltage (OPV) while IGBTs are ON. Two functions, a periodic Q_C discharger and recharger, and an overcurrent protection by V_{GE}, are added to the gate driver IC. While the IGBTs are ON, the periodic Q_C discharger and recharger periodically discharges and recharges Q_C. When V_{GE} dropped by each discharge is less than V_{REF}, it is detected as the overcurrent and the gate driver is forced to turn off to complete the overcurrent protection.

Fig. 2 shows a circuit schematics of the proposed gate driver IC with OPV. All circuits are integrated on a single chip except for the isolated power supplies. To achieve the two functions shown in blue in Fig. 1, an OPV circuit is added to our previously developed 6-bit current-source type digital gate driver [12, 13] with variable gate current (I_G) in 64 levels, where $I_G = n_{PMOS} \times 48$ mA and n_{PMOS} is an integer from 0 to 63 at turn-on. The 64-level I_G control is achieved by selectively turning on or off six pMOSFETs with binary weighted gate widths (W_P, $2W_P$, $4W_P$, $8W_P$, $16W_P$, $32W_P$) in the output stage depending on the 6-bit control signals for n_{PMOS} [12, 13]. The exact same is true for turn-off by controlling n_{NMOS}.

Fig. 3 shows a circuit schematics of the proposed OPV circuits. The OPV circuits include a digitally controlled oscillator (DCO) to determine charging and discharging time and a V_{GE} detector to detect the overcurrent by comparing V_{GE} and V_{REF}. The three outputs of the OPV circuits (Alarm,

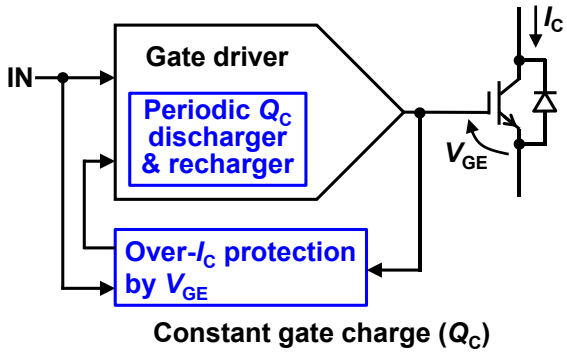

Fig. 1. Operation principle of proposed gate driver IC with fully integrated overcurrent protection function by measuring V_{GE} (OPV).

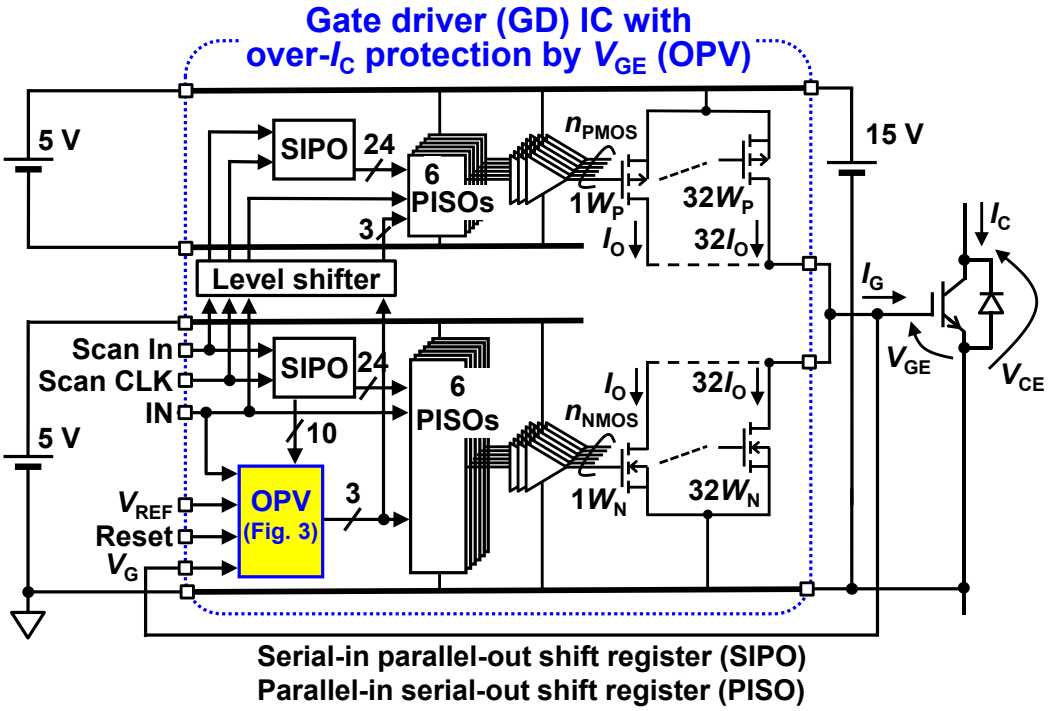

Fig. 2. Circuit schematics of proposed gate driver IC with OPV.

Internal_ONOFF, and Pulse) are fed into the low-side and high-side PISOs in Fig. 2.

Fig. 4 shows a circuit schematics of the V_{GE} detector. The V_{GE} detector includes an attenuator with an attenuation ratio of one-eighth to prevent the input gate voltage (V_G) from damaging the clocked comparator with overvoltage, and a low pass filter (LPF) with a cutoff frequency of 57 MHz to remove high-frequency ringing of V_G. When the attenuated and low pass filtered V_G drops below V_{REF}, Alarm output changes from low to high, forcing the IGBT to turn off.

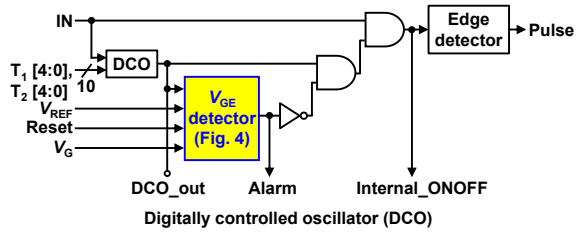

Fig. 3. Circuit schematics of proposed OPV circuits.

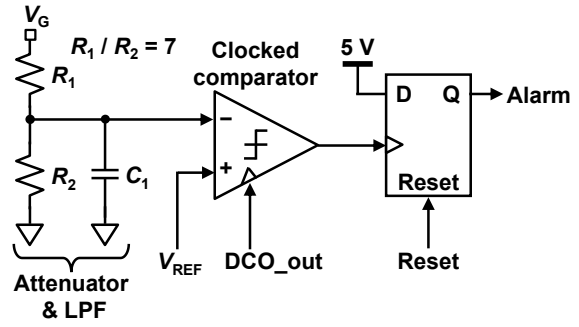

Fig. 4. Circuit schematics of V_{GE} detector.

Figs. 5 and 6 show the timing charts of the conventional and proposed overcurrent protection, respectively. Table I shows the design specifications of the four parameters (t_1, t_2, I_1, and I_2) that can be digitally controlled by this IC to achieve MGDC [11]. The discharging time (t_2) in MGDC is digitally controlled by 5-bit T_2 [4:0] of DCO from 0 s to 3.9 µs in 125 ns steps. The discharging gate current ($|I_2|$) in MGDC is digitally controlled by 6-bit I_2 [5:0] of the digital gate driver from 0 A to 3 A in 48 mA steps. Similarly, the charging time (t_1) in MGDC is digitally controlled by 5-bit T_1 [4:0] of DCO from 0 s to 19 µs in 625 ns steps. The charging gate current (I_1) in MGDC is digitally controlled by 6-bit I_1 [5:0] of the digital gate driver from 0 A to 3 A in 48 mA steps. All parameters are written in advance to the on-chip memory (two SIPOs in Fig. 2) by scan-in, eliminating the need for the high-speed digital signal generator to determine t_1 and t_2. In the conventional desaturation detection shown in Fig. 5, overcurrent is detected when V_{CE} exceeds a reference voltage (V_{REF}). In contrast, in MGDC shown in Fig. 6, Q_C (= $|I_2| \times t_2$) is periodically discharged with the $t_1 + t_2$ cycle, and if the resulting drop in V_{GE} is greater than V_{REF}, it is judged normal,

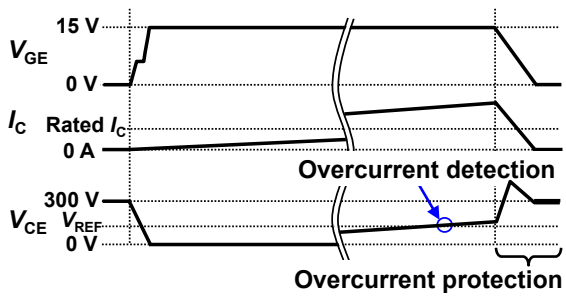

Fig. 5. Timing charts of conventional overcurrent protection.

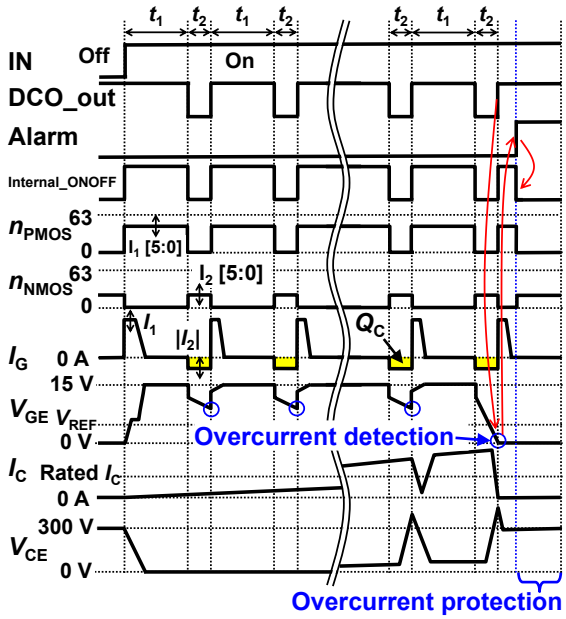

Fig. 6. Timing charts of proposed overcurrent protection using proposed gate driver IC shown in Fig. 2.

TABLE I. FOUR PARAMETERS FOR IC TO ACHIEVE MGDC

Parameters	Control bits	Range	Step
t_1	T_1 [4:0]	0 s to 19 µs	625 ns
t_2	T_2 [4:0]	0 s to 3.9 µs	125 ns
I_1	I_1 [5:0]	0 A to 3 A	48 mA
$\|I_2\|$	I_2 [5:0]	0 A to 3 A	48 mA

and if the resulting drop in V_{GE} is less than V_{REF}, it is judged overcurrent and the IGBTs are immediately turned off to protect from the overcurrent. In the t_1 period after each discharge, V_{GE} is recharged to 15 V.

Fig. 7 shows a die photo of the proposed gate driver IC with OPV fabricated with 180-nm BCD process. The die size is 2.0 mm by 2.5 mm.

III. MEASURED RESULTS

Figs. 8 and 9 show a circuit schematic and a photo of the measurement setup for a single-pulse test of an inductive load of 34 µH at 300 V for the IGBT module (FF100R12RT4, 1200 V rating) with a pulse rating of 200 A, respectively.

Figs. 10 and 11 show the measured waveforms of the conventional and proposed overcurrent protection, respectively. In the conventional desaturation detection in Fig. 10, the overcurrent is detected by the V_{CE} increases. In Fig. 10, the IGBT is turned off manually. In the proposed Fig. 11, where measured t_1 = 2.6 µs, t_2 = 0.51 µs, I_1 = 1.6 A, and $|I_2|$ = 0.62 A, "(1) Q_C discharge in t_2, (2) comparison of V_{GE} and V_{REF} at the end of t_2, and (3) recharge to V_{GE} = 15 V in t_1", is repeated in $t_1 + t_2$ cycles. When $V_{GE} < V_{REF}$, overcurrent (I_C = 370 A) is detected, Alarm changes from low to high, Internal_ONOFF changes from high to low, and the gate driver is forced to turn off to complete overcurrent protection. The delay from overcurrent detection to protection completion is 810 ns.

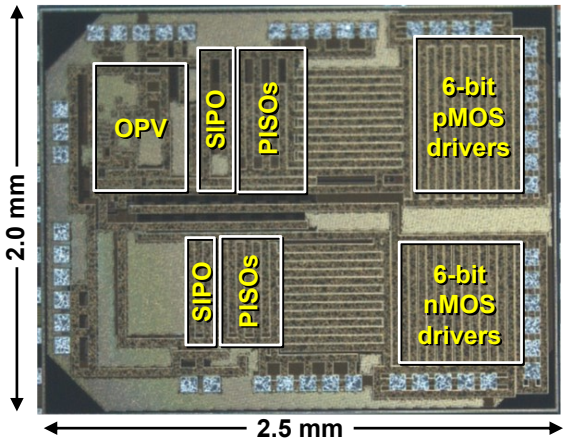

Fig. 7. Die photo of proposed gate driver IC with OPV fabricated with 180-nm BCD process.

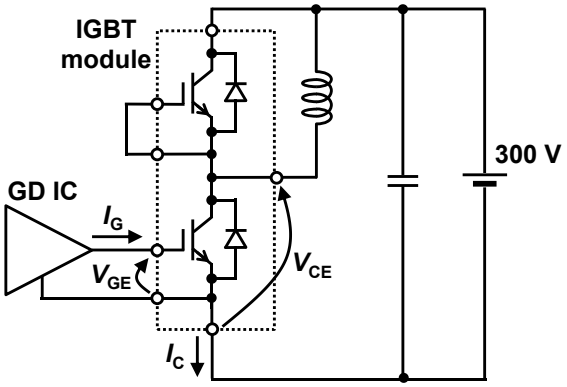

Fig. 8. Circuit schematic of single-pulse test.

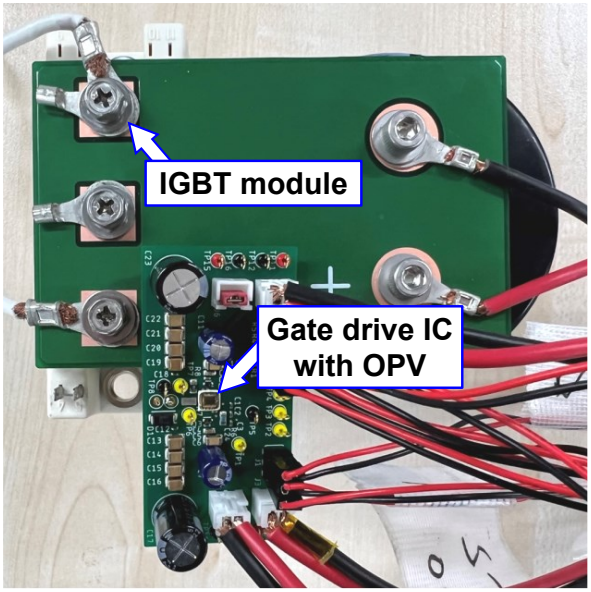

Fig. 9. Photo of measurement setup.

Table II shows a comparison table of overcurrent protection methods. This paper is the first work to fully integrate overcurrent protection into a gate driver IC without the need for external components such as high-voltage diodes.

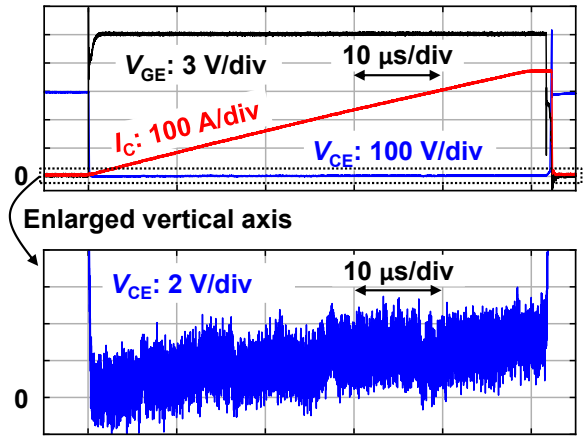

Fig. 10. Measured waveforms of conventional overcurrent protection.

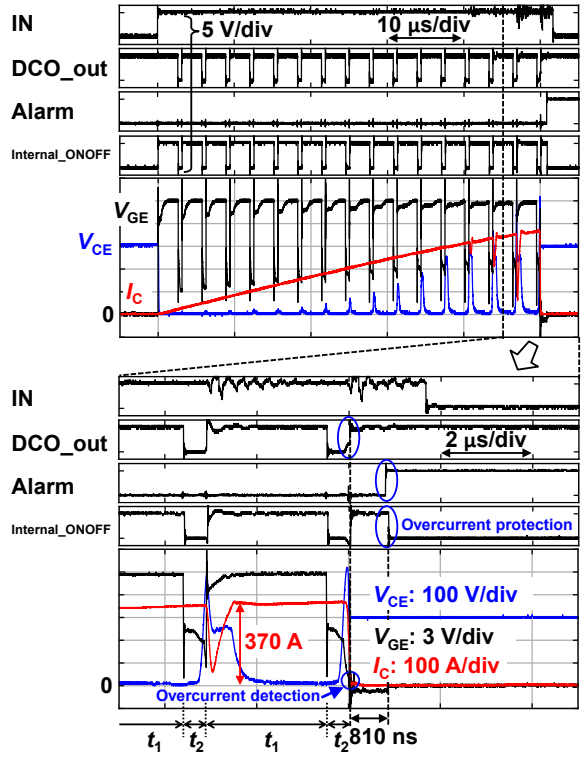

Fig. 11. Measured waveforms of proposed overcurrent protection using proposed gate driver IC.

IV. Conclusions

A gate driver IC with a fully integrated overcurrent protection function by measuring V_{GE} while IGBTs are ON is proposed. This paper is the first work to fully integrate overcurrent protection into a gate driver IC without the need for external components such as high-voltage diodes. In a single-pulse test of an inductive load at 300 V for an IGBT with a pulse rating of 200 A, the proposed gate driver IC fabricated with 180-nm BCD process successfully protected the overcurrent of 370 A with the protection delay of 810 ns.

Acknowledgment

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TABLE II. Comparison Table of Overcurrent Protection

Reference	[2-5]	[3, 6]	[8-9]	[10]	[11]	This work
Method	Current monitor	Desaturation	Gate charge	V_{GE} at Miller plateau	MGDC	MGDC
Measured value	I_C	V_{CE}	Q_G, V_{GE}	V_{GE}	V_{GE}	V_{GE}
Measurement from gate terminal	No	No	Yes	Yes	Yes	Yes
Overcurrent detection during ON	Yes	Yes	No	No	Yes	Yes
Fully integrated overcurrent protection function	No	No	No	No	No	Yes
Protection delay [ns]	22 [2] 100 [3]	250 [3] 400 [6]	200	500	N/A	810
Additional circuits except comparators	Current sensor	High voltage diode	Integrator	Filter	Q_C discharger	Q_C discharger, DCO

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